

## WHAT IS CLAIMED IS:

1 1. A computer implemented method of multilevel dither  
2 screening comprising the steps of:

3 defining a dither value for each pixel of a screening  
4 matrix;

5 packing plural pixel values corresponding to plural  
6 pixels into equal sections of a first data word;

7 packing plural corresponding dither values into said  
8 equal sections of a second data word;

9 adding corresponding sections said first data word and  
10 said second data word in an arithmetic logic unit selectively  
11 spilttable into said equal sections forming a sum data word;

12 saturating any section of said sum data word generating  
13 an carry output during addition to a section of all 1's  
14 forming a saturated sum data word; and

15 truncating a predetermined number of least significant  
16 bits of each section of said saturated sum data word forming  
17 a dither screen data word.

1 2. The method of claim 1, wherein:

2 said step of adding corresponding sections said first  
3 data word and said second data word further includes saving a  
4 carry out of each section in a multiple flags data word;

5 said step of saturating any section of said sum data word  
6 generating an carry output during addition includes

7 expanding said carry out of each section in said  
8 multiple flags data word to fill a corresponding section  
9 of a mask data word,

12/30/99

10 forming the logical OR of (1) a logical AND of a  
11 saturated data word having all 1's in every section and  
12 said mask data word, and (2) a logical AND of said sum  
13 data word and a logical inverse of said mask data word.

1 3. The method of claim 1, wherein:  
2 said step of truncating a predetermined number of least  
3 significant bits of each section of said saturated sum data  
4 word includes  
5 right shifting said saturated sum data word said  
6 predetermined number of bits,  
7 forming a mask data word having said predetermined  
8 number of 1's in least significant bits of each section  
9 and 0's in most significant bits of each section, and  
10 forming a logical AND of said shifted saturated sum  
11 data word and said mask data word.

1 4. The method of claim 1, wherein:  
2 said input pixel values are represented in a fixed point  
3 format of 8 bits including 4 integer bits and 4 fractional  
4 bits;  
5 said dither values are represented in a fixed point  
6 format of 4 bits including zero integer bits and 4 fractional  
7 bits; and  
8 said predetermined number of bits is 4.

1 5. The method of claim 1, further comprising the step  
2 of:  
3 quantizing each section of said dither screen data word  
4 into a limited set of threshold ranges.

1        6. A printer comprising:  
2        a transceiver adapted for bidirectional communication  
3 with a communications channel;  
4        a memory;  
5        a print engine adapted for placing color dots on a  
6 printed page according to received image data and control  
7 signals; and  
8        a programmable data processor connected to said  
9 transceiver, said memory and said print engine, said  
10 programmable data processor including a selectively splittable  
11 arithmetic logic unit, said programmable data processor  
12 programmed to:  
13            receive print data corresponding to pages to be  
14 printed from the communications channel via said  
15 transceiver;  
16            convert said print data into image data and control  
17 signals for supply to said print engine for printing a  
18 corresponding page, said conversion including multilevel  
19 dither screening by  
20            defining a dither value for each pixel of a  
21 screening matrix,  
22            packing plural pixel values corresponding to plural  
23 pixels into equal sections of a first data word,  
24            packing plural corresponding dither values into  
25 said equal sections of a second data word,  
26            adding corresponding sections said first data word  
27 and said second data word in said arithmetic logic  
28 selectively spilt into said equal sections forming a sum  
29 data word,

30 saturating any section of said sum data word  
31 generating an carry output during addition to a section  
32 of all 1's forming a saturated sum data word, and  
33 truncating a predetermined number of least  
34 significant bits of each section of said saturated sum  
35 data word forming a dither screen data word.

1 7. The printer of claim 6, wherein:  
2 said programmable data processor further including  
3 a multiple flags register connected to said  
4 arithmetic logic unit receiving and storing a carry out  
5 from each of said sections of said arithmetic logic unit,  
6 and  
7 an expand circuit connected to said multiple flags  
8 register for expanding each bit of said multiple flags  
9 register to fill a corresponding section thereby forming  
10 a mask data word; and  
11 wherein said programmable data processor is programmed to  
12 saturate any section of said sum data word generating an carry  
13 output during addition by  
14 forming in said arithmetic logic unit the logical  
15 OR of (1) a logical AND of a saturated data word having  
16 all 1's in every section and said mask data word, and (2)  
17 a logical AND of said sum data word and a logical inverse  
18 of said mask data word.

1 8. The printer of claim 6, wherein:  
2 said programmable data processor further including  
3 a selectable shifter,

4           a mask generator having an input and an output  
5       filling each section with a number of least significant  
6       1's equal to a number at said input and  
7       wherein said programmable data processor is programmed to  
8       truncating a predetermined number of least significant bits of  
9       each section of said saturated sum data word by  
10           supplying said predetermined number to said shifter  
11       to right shift said saturated sum data word by said  
12       predetermined number of bits,  
13           supplying said predetermined number to said input  
14       of said mask generator thereby forming a mask data word  
15       having said predetermined number of 1's in least  
16       significant bits of each section and 0's in most  
17       significant bits of each section, and  
18           forming in said arithmetic logic unit a logical AND  
19       of said shifted saturated sum data word and said mask  
20       data word.

005F1=SHIFTER